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10EC/TE71

Seventh Semester B.E. Degree Examination, Dec.2014/Jan.2015
Computer Communication Networks

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Discuss the TCP/IP model with functionalities of each layer. Consider source destination and intermediate modes for discussion. **(10 Marks)**

b. Explain the different services provided by telephone networks. **(04 Marks)**

c. Describe four levels of addressing used in internet (TCP/IP) with examples. **(06 Marks)**

2 a. What is HDLC? Explain different frame formats with control field used by HDLC. **(10 Marks)**

b. A system uses stop-and-wait ARQ protocol. If each packet carries 2000bits of data, how long does it take to send 1 million bits of data if the speed is 2×10^8 m/sec? Ignore transmission, waiting and processing delays. We assume no data or control frame is lost or damaged. Repeat for go-back-n with window) size = 7. **(10 Marks)**

3 a. What is channelization in the context of multiple access? What are various channelization techniques? Explain CDMA technique. **(10 Marks)**

b. Two stations A and C are connected to a shared channel with data rate 10Mbps. The distance between A and C is 2500m and the propogation speed is 2×10^8 m/s. Station A starts sending a long frame at time $t_1 = 0$; station C starts sending a long frame at time $t_2 = 3\mu$sec. The size of the frame is long enough to guarantee the detection of collision by both stations, Find: i) The time when station C hears the collision (t_3); ii) Time when station A hears the collision (t_4); iii) The number of bits A has sent before detecting the collision; iv) The number of bits C has sent before detecting the collision. **(10 Marks)**

4 a. Explain the MAC frame format of IEEE802.3. Write a note on frame length. **(10 Marks)**

b. Explain the features of MAC sublayer and physical layer of Gigabit Ethernet. **(10 Marks)**

PART – B

5 a. Briefly explain the three criteria's of a transparent bridge with example. **(10 Marks)**

b. Explain the following connecting devices: i) Passive hub; ii) Repeater; iii) Bridge; iv) Router; v) Gateway. **(10 Marks)**

6 a. What is NAT? Explain how address translation is done in NAT. **(09 Marks)**

b. Why IPV4 to IPV6 transition is required? What are various techniques used in transition? Explain them. **(08 Marks)**

c. Bring out any 3 differences between IPV4 and IPV6 addressing schemes. **(03 Marks)**

7 a. Explain distance vector routing with an example. **(10 Marks)**

b. With a neat flow chart explain Dijkstra algorithm for the network shown in Fig.Q.7(b). Assume 'A' as root node. Mention the routing table for root A. Refer Fig.Q.7(b). **(10 Marks)**

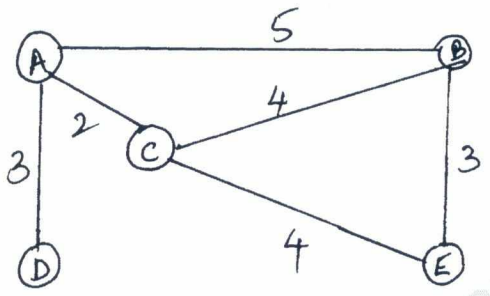

Fig.Q.7(b)

8 a. How is TCP better than UDP? Explain services offered by TCP. **(10 Marks)**

b. What is Name Space? How is it classified? What is DNS? **(10 Marks)**

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10EC/TE72

Seventh Semester B.E. Degree Examination, Dec.2014/Jan.2015
Optical Fiber Communication

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. With neat sketches of RI profile and wave propagation in optical fiber communication, compare different types of fibers? **(08 Marks)**

b. With neat sketches, explain the characteristics and operating ranges of the four key optical fiber link components. **(07 Marks)**

c. Explain MCVD process for manufacturing low loss GI fiber. **(05 Marks)**

2 a. Explain different types of attenuation in optical fiber. **(06 Marks)**

b. Classify and explain chromatic dispersion within a single mode fiber. **(08 Marks)**

c. Consider a 10 km long multimode in which $n_1 = 1.483$ and $\Delta = 0.01$. Calculate n_2 and pulse broadning after travelling 10 km. **(06 Marks)**

3 a. Explain with schematic an LED which is highly directional and sketch the spectral emission pattern of an LED. **(07 Marks)**

b. Compare operating parameters of G_e, S_i and InGaAs of PIN and APD. **(07 Marks)**

c. With neat sketch, explain RAPD structure and the electrical fields. **(06 Marks)**

4 a. Explain different types of fiber splicing methods used for optical fibers. Explain electric arc fusion splicing. **(08 Marks)**

b. Explain expanded beam fiber optic connector. **(05 Marks)**

c. List several possible lensing scheme and explain briefly non imaging lensing scheme. **(07 Marks)**

PART – B

5 a. Draw a signal path through a digital link with relevant components and optical/electrical waveforms at every stage. **(06 Marks)**

b. What are the noise sources and disturbances that arise in optical pulse detection mechanism? Explain them in detail. **(06 Marks)**

c. Draw and explain eye pattern and mark the fundamental measurement parameter. **(08 Marks)**

6 a. What is rise time budget? Explain its significance. Derive an expression for the system rise time budget in terms of transmitter, fiber and receiver rise time. **(08 Marks)**

b. Explain subcarrier multiplexing, with neat block diagram. **(05 Marks)**

c. Derive an expression for the CNR of an analog communication system under limiting condition of noise sources involved. **(07 Marks)**

7 a. Explain WDM networks containing various types of optical amplifiers. **(07 Marks)**

b. Write a note on MZI multiplexer. **(07 Marks)**

c. Explain dielectric thin film filter and its applications. **(06 Marks)**

8 a. With neat energy level diagram, explain EDFA. **(10 Marks)**

b. Write a note on :

i) Basic format of

STS – N – SONET and

STM – N – SDH frame

ii) High speed light wave links. **(10 Marks)**

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10EC73

Seventh Semester B.E. Degree Examination, Dec.2014/Jan.2015
Power Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Mention any four properties of a super power device should possess. **(02 Marks)**

b. What is a converter? How are power converters classified? Explain briefly. **(08 Marks)**

c. Mention some important advantages and disadvantages of power converters. **(04 Marks)**

d. What are the peripheral effects of power electronics converters and how they are overcome? **(06 Marks)**

2 a. The collector clamping circuit of Fig.Q.2(a) has the following parameters: V_{BB} = 14V, R_B = 3Ω, β = 15, V_{BE} = 0.7V, V_{D2} = 0.9V, V_{D1} = 2.1V, R_C = 2Ω, V_{CC} = 120V, Find: i) Collector current without clamping; ii) Collector-emitter clamping voltage; iii) Collector current with clamping. **(05 Marks)**

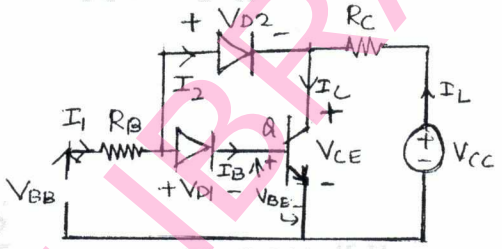

Fig.Q.2(a)

b. Draw the switching model of MOSFET and explain its switching characteristics with neat figure. **(06 Marks)**

c. What is an IGBT? Compare IGBT with BJT and MOSFET. **(05 Marks)**

d. Why isolation is needed? Explain the two methods of isolation. **(04 Marks)**

3 a. With a neat figure explain the dynamic turn-on and turn-off characteristics of a thyristor. **(08 Marks)**

b. Briefly explain di/dt and dv/dt protection of SCR. **(06 Marks)**

c. Design a UJT relaxation oscillator for triggering an SCR, with UJT having the following parameters η = 0.72, I_P = 60μA, I_V = 4mA, V_v = 2.5V, V_{BB} = 15V, R_{BB} = 5KΩ, leakage current with emitter open is 3mA. Also calculate minimum and maximum value of RC variable resistance). **(06 Marks)**

4 a. With a circuit diagram and waveforms explain the working of a single phase semi controlled rectifier. Derive an expression for the average voltage across the R-L load. **(08 Marks)**

b. For a single phase fully controlled bridge rectifier with highly inductive load and continuous current, obtain average load voltage and current if the load resistance is 10Ω and firing angle is 45°, and is fed from 230V, 50Hz supply. Draw the load voltage waveform and supply current waveform. **(06 Marks)**

c. What is a dual converter? Explain its operation with a neat circuit diagram. **(06 Marks)**

PART – B

5 a. State the conditions to be satisfied for proper turn-off of SCR. **(02 Marks)**

b. With the help of circuit diagram and waveforms explain the operation of self commutation. **(06 Marks)**

c. In the Fig.Q.5(c) the source voltage V_s = 100V and the current through R_1 and R_2 is 25A. The turn off time of both the SCRs is 40μsec. Find the value of capacitor for successful commutation and hence show that circuit turn off time is 0.693 RC. **(08 Marks)**

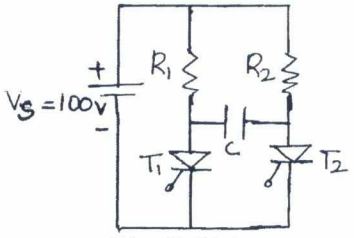

Fig.Q.5(c)

d. In the auxiliary commutation circuit shown in Fig.Q.5(d) the battery voltage is 100V. Maximum load current is 40A and thyristor turn off time is 40μsec. Assume 50% tolerance on turn off time. Find L and C of the commutation circuit. **(04 Marks)**

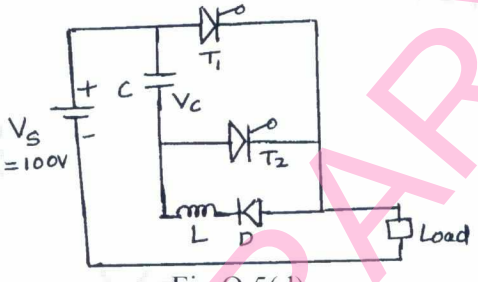

Fig.Q.5(d)

6 a. Distinguish between on-off control and phase control of AC voltage controller. **(04 Marks)**

b. Explain the operation of single phase bidirectional AC voltage controller for inductive load with the help of circuit diagram and waveforms. **(06 Marks)**

c. An AC voltage controller has a resistive load of R = 10Ω, and RMS input voltage is V_S = 120V, 50Hz. The thyristor switch is on for n = 25 cycles and off form = 75 cycles. Find: i) rms output voltage; ii) Input power factor; iii) Average and RMS thyristor current and hence derive the above expressions for V_{orm} and PF. **(10 Marks)**

7 a. Explain the working principle of step-down chopper and derive expression for i) Average output voltage; ii) Output power; iii) Effective input resistance in terms of chopper duty cycle. **(08 Marks)**

b. With the help of a circuit diagram, explain four quadrant type E choppers. **(08 Marks)**

c. A step up chopper has input voltage of 220V and output voltage of 660V. If the non conducting time of the thyristor is 100μsec, compute the pulse width of the output voltage. If the pulse width is halved for constant frequency operation, find new output voltage. **(04 Marks)**

8 a. Explain a single phase full bridge inverter with relevant circuit diagram and waveforms. Assume R-L load. **(08 Marks)**

b. With the help of circuit diagram and wave forms explain the operation of transistorized CSI (current source inverter). What are the advantages and disadvantages of CSI? **(08 Marks)**

c. The single phase half bridge inverter has the DC input of 48V. The load resistance is 4.8Ω. Determine: i) RMS value of the output voltage; ii) RMS value of the fundamental component; iii) Total harmonic distortion. **(04 Marks)**

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10EC74

Seventh Semester B.E. Degree Examination, Dec.2014/Jan.2015
Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain :
   i) Embedded system
   ii) Hard RTS
   iii) Watch dog timer. **(06 Marks)**

   b. With a block diagram, explain briefly the various components in a microprocessor based embedded system. **(07 Marks)**

   c. Briefly describe the major elements of the embedded system development life cycle. **(07 Marks)**

2 a. Explain direct and register indirect addressing modes with diagram. Also write the timing diagram for serial write operation with an 8 bit register. **(06 Marks)**

   b. Compare :
   i) Big Endian and little Endian formats
   ii) RISC and CISC registers
   iii) Truncation and rounding errors. **(06 Marks)**

   c. Explain the direct mapping cache management strategy with an example. What are the trade off between write through and delayed write algorithm? **(08 Marks)**

3 a. Explain the internal diagram of SRAM and write timing diagram for read operation. **(06 Marks)**

   b. Write the inside and outside diagrams for DRAM along with read and write operations. **(08 Marks)**

   c. Explain Associative mapping cache implementation. **(06 Marks)**

4 a. Write the flow diagrams for waterfall and V lifecycle models and briefly explain waterfall steps. **(06 Marks)**

   b. Write a hardware architecture and data and counter flow diagram of a counter system and explain briefly flow diagram. **(08 Marks)**

   c. Explain the characterizing and identifying the requirements of a system, with respect to a digital counter. **(06 Marks)**

PART – B

5 a. Discuss task control block. Mention some of the major components of task control block. **(05 Marks)**

   b. Differentiate between :
   i) Program and process
   ii) Processes and threads
   iii) Light weighted and heavy weighted threads. **(06 Marks)**

   c. Explain the different functions of embedded operating. **(09 Marks)**

6 a. Discuss foreground/ background system. Mention the difference between foreground and background task. **(06 Marks)**

b. Describe virtual model and high level model for OS architectures. **(06 Marks)**

c. Write the algorithm for a simple OS kernel, using C language notation for 3 asynchronous tasks using TCB's only. The 3 tasks use a common data buffer for read, increment and display operations. **(08 Marks)**

7 a. Write the Amdahl's limitation for performance improvement/optimization. Consider a system with the following characteristics. The task to be analysed and improved currently executes in 100 time units, and the goal is to reduce execution time to 50 units, the algorithm to be improved uses 40 time units. Determine the unknown parameter and write the inference. **(06 Marks)**

b. Describe the methods by which we can perform a time coding analysis of an embedded a time coding analysis of an embedded application. Discuss the advantages and disadvantages of each. **(08 Marks)**

c. Write 'C' functions to determine the sum of the elements in an array and analyze it line by line for its time complexity. **(06 Marks)**

8 a. Describe memory loading with equation, figure and an example. **(08 Marks)**

b. Write short notes on the following :

i) Tricks of the trade

ii) Performance optimization. **(12 Marks)**

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10EC751

Seventh Semester B.E. Degree Examination, Dec.2014/Jan.2015
DSP Algorithms & Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain a digital signal processing system with the help of a block diagram. **(07 Marks)**

b. List the major unique architectural features implemented in any programmable DSP devices. **(03 Marks)**

c. Derive the relationship between DFT and frequency response and also define frequency resolution and signal record length. **(06 Marks)**

d. An FFT is employed for determining the frequency components of a random signal. It is required that the resolution of FFT to be <=5 Hz, for a signal with f_{max} = 1.25 kHz. Determine i) Sampling interval, TS.
ii) FFT length (N) as a power of 2.
iii) Minimum signal record length. **(04 Marks)**

2 a. Draw the structure of a 4×4 Braun multiplier and also explain its operation. **(08 Marks)**

b. Explain the pointer updating algorithm for circular addressing mode. **(08 Marks)**

c. Compute the sequence in which the input data should be ordered for a 16 point DIT FFT using Bit reversed addressing mode. **(04 Marks)**

3 a. Describe the following units of TMS320C54XX processor: i) Barrel shifter ii) Central processing unit. **(08 Marks)**

b. What is meant by addressing mode? Explain the absolute, accumulator, direct and indirect addressing modes of TMS320C54XX DSP processor. **(12 Marks)**

4 a. Describe the operation of the following instructions:
i) MAC *AR3-, *AR4+, B, A
ii) MAS *AR3-, *AR+, B, A
iii) RPTZ and RPTB. **(06 Marks)**

b. Explain the hardware timer of TMS320C54XX DSP with logical block diagram. **(07 Marks)**

c. Explain the pipe line operation of TMS320C54XX processor. **(07 Marks)**

PART – B

5 a. What is the significance of Q-notation in DSP? **(04 Marks)**

b. Represent each of the following numbers in desired Q-notation format:
i) -352 as Q_0 number.
ii) 3.125 as Q_7 number.
iii) BDAFh in Q_7 and Q_{15} number.
iv) -0.160123 as Q_{15} number.
v) 4400h as Q_0 number. **(06 Marks)**

c. Explain with the help of block diagram and mathematical equations implementation of decimation filter on TMS320C54XX processor. **(10 Marks)**

6 a. What minimum size FFT must be used to compute 500 points DFT? What must be done to the samples before the chosen FFT is applied? **(04 Marks)**

b. Derive the optimum scaling factor for the DIT FFT butterfly. **(08 Marks)**

c. Write an assembly language program for implementing following on TMS320C54XX processor:

i) Bit reversed address generation

ii) Spectrum of the transformed data. **(08 Marks)**

7 a. What is an interrupt? With a neat flow chart explain handling of interrupt by TMS320C54XX processor. **(10 Marks)**

b. How does DMA help in increasing the speed of a DSP processor and also explain register sub addressing technique for configuring DMA. **(10 Marks)**

8 a. With neat block diagram explain the DSP based biotelemetry receiver. **(10 Marks)**

b. With neat block diagram explain the CODEC interface circuit. **(10 Marks)**

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10EC/TE762

Seventh Semester B.E. Degree Examination, Dec.2014/Jan.2015

Real Time Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Classify RTS based on time constraints. **(06 Marks)**

b. Explain the following:
i) Clock based tasks ii) Event based tasks iii) Interactive system **(06 Marks)**

c. Differentiate real time systems and non-real time systems. **(02 Marks)**

d. Explain the following program types: i) Multi-tasking; ii) Real time. **(06 Marks)**

2 a. Explain sequence control for a single chemical reactor vessel, with neat sketch. **(06 Marks)**

b. With neat diagram, explain loop control and give the advantages of DDC over analog control. **(08 Marks)**

c. With neat sketch, explain hierarchical systems. **(06 Marks)**

3 a. With a diagram, explain digital input interface. **(06 Marks)**

b. Explain with a neat diagram analog output system. **(05 Marks)**

c. Draw single chip computer and explain. **(03 Marks)**

d. Explain communications and the ways of characterizing serial communication techniques. **(06 Marks)**

4 a. Explain the following: i) Security, ii) Readability, iii) Portability **(09 Marks)**

b. Explain exception handling. **(06 Marks)**

c. Explain co-routines. **(05 Marks)**

PART – B

5 a. With neat diagram explain priority structures. **(07 Marks)**

b. Explain scheduling strategies. **(05 Marks)**

c. Give the basic functions of task management. Explain task states with a typical task diagram. **(08 Marks)**

6 a. With a diagram, explain task chaining and swapping. **(05 Marks)**

b. Draw the figure for: i) non partitioned, ii) partitioned memory. **(02 Marks)**

c. Explain semaphore. **(05 Marks)**

d. What is Liveness? Explain. **(08 Marks)**

7 a. Explain software design in case of preliminary design of RTSS with diagram. **(08 Marks)**

b. With flow-chart explain foreground/background approach. **(08 Marks)**

c. Explain multi-tasking approach. **(04 Marks)**

8 a. Explain Yourdon methodology. **(05 Marks)**

b. Draw and explain context diagram for drying oven in case of ward and Mellor method. **(08 Marks)**

c. Differentiate between Ward & Mellor and Hatley & Pirbhai methodologies. **(02 Marks)**

d. Explain the architecture model in case of Hatley and Pirbhai method. **(05 Marks)**

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